

## CLAIMS

1           1. A method of processing a semiconductor structure comprising:  
2           providing a substrate;  
3           depositing a lattice-mismatched first layer on said substrate;  
4           annealing said first layer at a temperature greater than 100°C above the deposition  
5           temperature; and  
6           depositing a second layer on said first layer with a greater lattice mismatch to said  
7           substrate than said first layer.

1           2. The method of claim 1, wherein said substrate has at least a surface layer comprising  
2           Si and said first and second layers comprise  $\text{Si}_{1-x}\text{Ge}_x$ .

1           3. The method of claim 1, wherein said substrate has at least a surface layer comprising  
2           GaAs and said first and second layers comprise  $\text{In}_y\text{Ga}_{1-y}\text{As}$ .

1           4. The method of claim 1, wherein said substrate has at least a surface layer comprising  
2           GaP and said first and second layers comprise  $\text{In}_z\text{Ga}_{1-z}\text{P}$ .

1           5. The method of claim 2, wherein said first and second layers differ by a Ge  
2           concentration less than 10% Ge.

1           6. The method of claim 2, wherein said first and second layers differ in Ge concentration

2 by approximately 1.5% Ge.

1 7. The method of claim 2, wherein said first and second layers of  $\text{Si}_{1-x}\text{Ge}_x$  are deposited  
2 at a growth temperature less than 850°C.

1 8. The method of claim 2, wherein said annealing occurs at a temperature greater than  
2 900°C.

1 9. The method of claim 2, wherein anneal time is greater than 0.1 seconds.

1 10. The method of claim 2, wherein said first and second layers differ in Ge  
2 concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the  
3 anneal temperature is approximately 1050°C.

1 11. The method of claim 2, wherein said first and second layers differ in Ge  
2 concentration by approximately 1.5%, the growth temperature is approximately 750°C, and the  
3 anneal temperature is approximately 1050°C, and the anneal time is greater than 0.1 seconds.

1 12. The method of claim 1, wherein said lattice-mismatched semiconductor layer is  
2 deposited by chemical vapor deposition.

1 13. A method of processing a semiconductor graded composition layer structure on a

semiconductor substrate comprising:

providing a semiconductor substrate;

depositing a first layer having a series of lattice-mismatched semiconductor layers on said substrate;

annealing said layer at a temperature greater than 100°C above the deposition temperature;

depositing a second layer on said first layer with a greater lattice mismatch to said substrate than said first layer; and

annealing said second layer at a temperature greater than 100°C above the deposition temperature of said second layer.

14. The method of claim 13, wherein said substrate has at least a surface layer comprising Si and said first and second layers comprise  $\text{Si}_{1-x}\text{Ge}_x$ .

15. The method of claim 13, wherein said substrate has at least a surface layer comprising GaAs and said first and second layers comprise  $\text{In}_y\text{Ga}_{1-y}\text{As}$ .

16. The method of claim 13, wherein said substrate has at least a surface layer comprising GaP and said first and second layers comprise  $\text{In}_z\text{Ga}_{1-z}\text{P}$ .

17. The method of claim 14, wherein sequential layers in the graded composition layers differ by a Ge concentration less than 10% Ge.

1 18. The method of claim 14, wherein sequential layers in the graded composition layers  
2 differ in Ge concentration by approximately 1.5% Ge.

1 19. The method of claim 14, wherein said first layer and second layers are deposited at a  
2 growth temperature of less than 850°C.

1 20. The method of claim 14, wherein said annealing occurs at a temperature greater than  
2 900°C.

1 21. The method of claim 14, wherein anneal time is greater than 0.1 seconds.

1 22. The method of claim 14, wherein sequential layers in the graded composition layers  
2 differ in Ge concentration by approximately 1.5%, the growth temperature is approximately  
3 750°C, and the anneal temperature is approximately 1050°C.

1 23. The method of claim 14, wherein sequential layers in the graded composition layers  
2 differ in Ge concentration by approximately 1.5%, the growth temperature is approximately  
3 750°C, and the anneal temperature is approximately 1050°C, and the anneal time is greater than  
4 0.1 seconds.

1 24. The method of claim 13, wherein said lattice-mismatched semiconductor layer is  
2 deposited by chemical vapor deposition.